佳恩半导体 JIAENSEMI

JFPC9N50C
JFFM9N50C

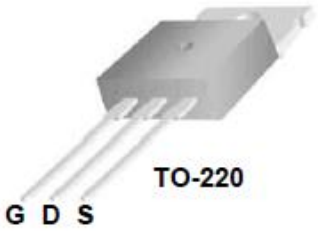
500V N-Channel MOSFET

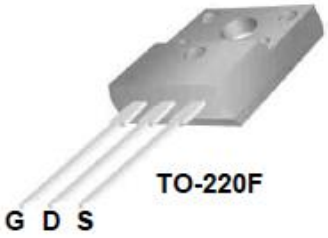
General Description

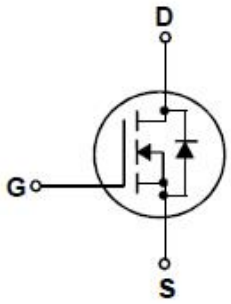
This Power MOSFET is produced using advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 9A, 500V, RDS(on)typ. = 0.85Ω@VGS = 10 V
- Low gate charge
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability







Absolute Maximum Ratings T_C = 25 ℃ unless otherwise noted

Symbol	Parameter		JFPC9N50C	JFFM9N50C	Units
V_{DSS}	Drain – Source Voltage		500		V
I_D	Drain Current	Continuous (T_C = 25 ℃)	9	9*	A
		Continuous (T_C = 100 ℃)	5.1	5.1*	A
I_{CM}	Drain Current - Pulsed	(Note 1)	32		A
V_{GSS}	Gate – Source Voltage		±30		V
EAS	Single Pulsed Avalanche Energy	(Note 2)	510		mJ
I_{AR}	Avalanche Current	(Note 1)	8		A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	19.2		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5		V/ns
P_D	Power Dissipation (T_C = 25 ℃)		192	40	W
	-Derate above 25 ℃		1.53	0.32	W/℃
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to +150		℃
T_L	Maximum lead temperature for soldering purposes 1/8" frome case for 5 seconds		300		℃

*Drain current limited by maximum junction temperature.

Thermal characteristics

Symbol	Parameter	JFPC9N50C	JFFM9N50C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.65	3.15	℃/W
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	℃/W

Electrical Characteristics T_C = 25 ℃ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain – Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	500	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 uA, Referenced to 25℃	--	0.6	--	V/℃
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	uA
		V_{DS} = 400 V, Tc = 125 ℃	--	--	10	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{GS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{GS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source on-Resistance	V_{GS} = 10V, I_D = 4.5 A	--	0.73	0.9	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 4.5 A (Note 4)	--	6.8	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1121	--	pF
C_{oss}	Output Capacitance		--	96	--	pF
C_{rss}	Reverse Transfer Capacitance		--	5.5	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 250 V, I_D = 9.0 A , V_{GS} = 10 V, R_G = 25Ω (Note 4,5)	--	18	--	ns
t_r	Turn-On Rise Time		--	22	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	40	--	ns
t_f	Turn-Off Fall Time		--	19	--	ns
Q_g	Total Gate Charge	V_{DS} = 250 V, I_D = 9.0 A V_{GS} = 10 V (Note 4,5)	--	24	--	nC
Q_{gs}	Gate-Source Charge		--	5.1	--	nC
Q_{gd}	Gate-Drain Charge		--	9.5	--	nC
Drain – Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	9	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	32	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 9.0 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 9.0 A dI_F/dt = 100 A/us (Note 4)	--	363	--	ns
Q_{rr}	Reverse Recovery Charge		--	1.92	--	uC

Notes:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature
2. L = 3mH , I_{AS} = 9.0A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25℃
3. I_{SD} ≤ 9.0A, di/dt ≤ 100A/us, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulsed Test : Pulsed width ≤300us, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

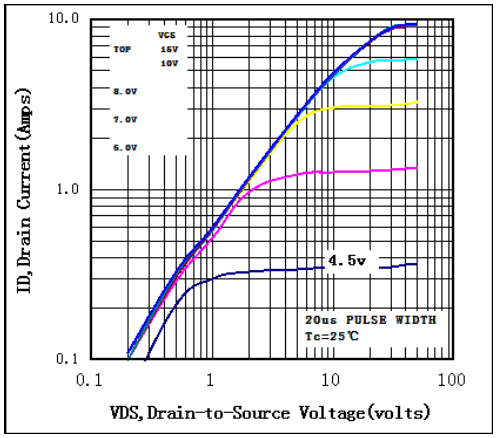


Figure 1. 输出特性曲线, Tc=25℃

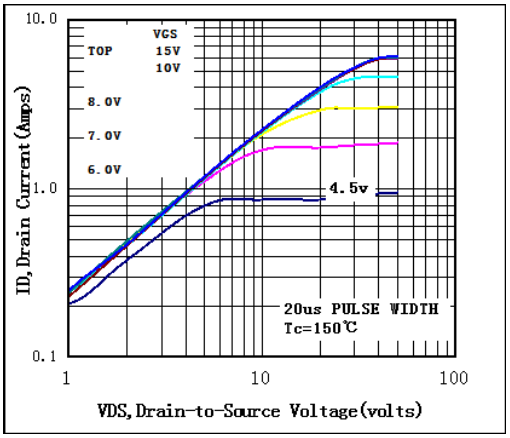


Figure 2. 输出特性曲线, Tc=150℃

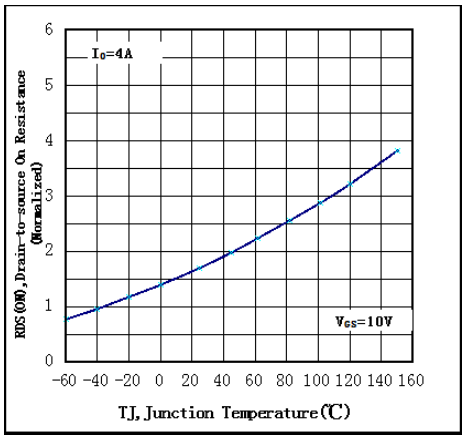


Figure 3. 归一化导通电阻与温度曲线

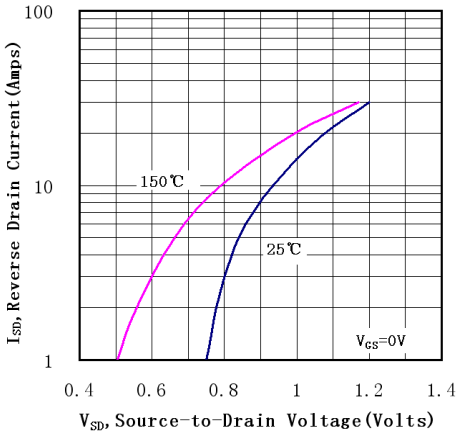


Figure 4. 二极管正向电压曲线

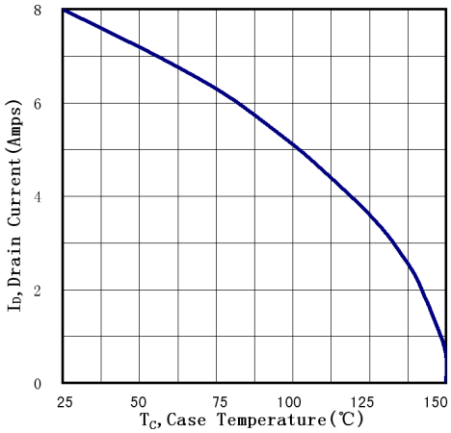


Figure 5. 最大漏极电流与壳温曲线

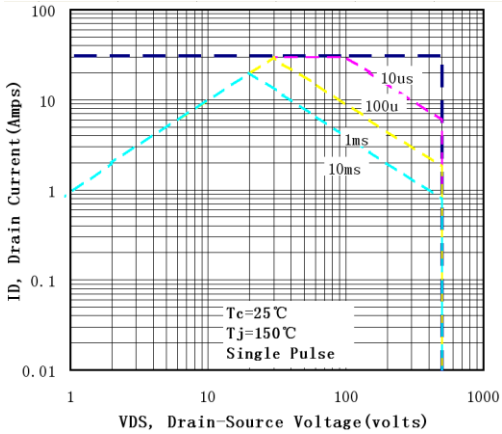


Figure 6. 最大安全工作区域

Typical Characteristics

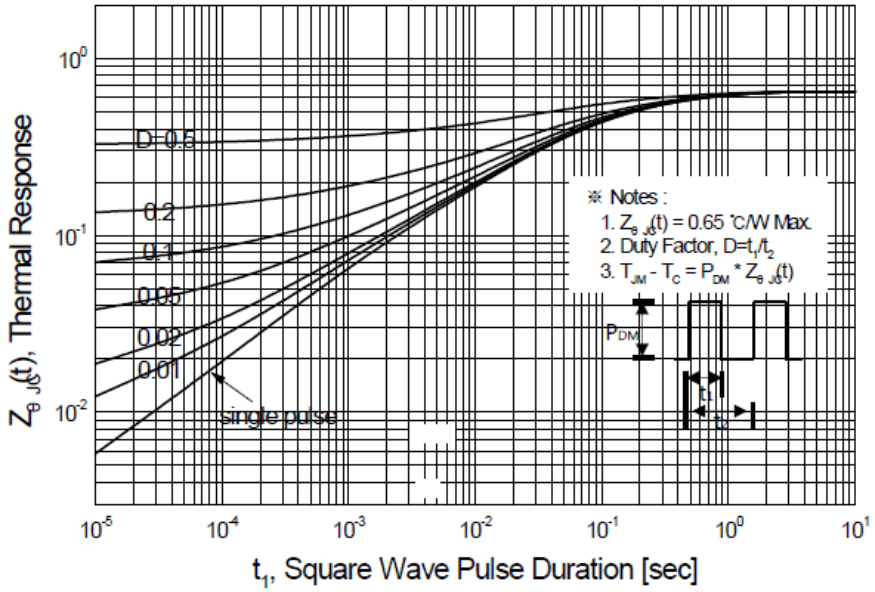


Figure 11-1. Transient Thermal Response Curve for JFPC9N50C

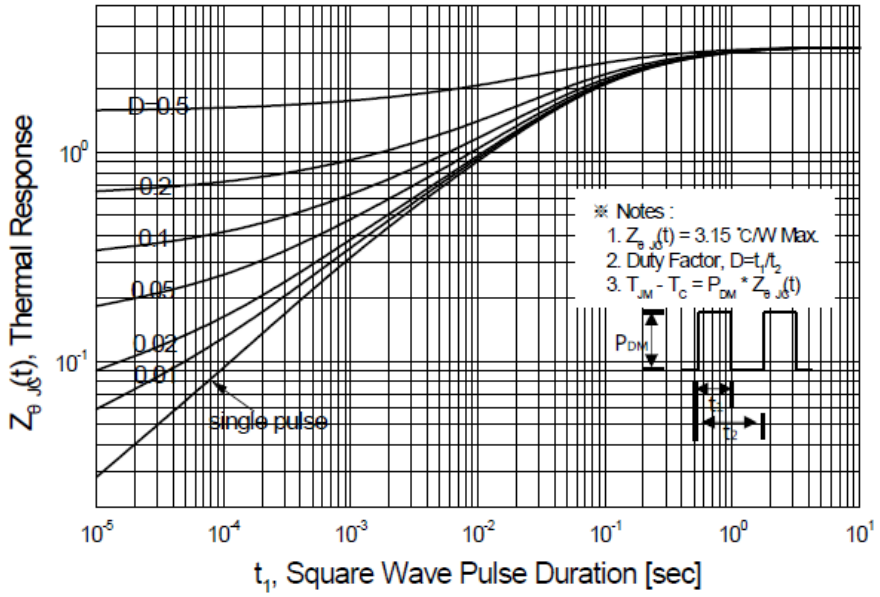
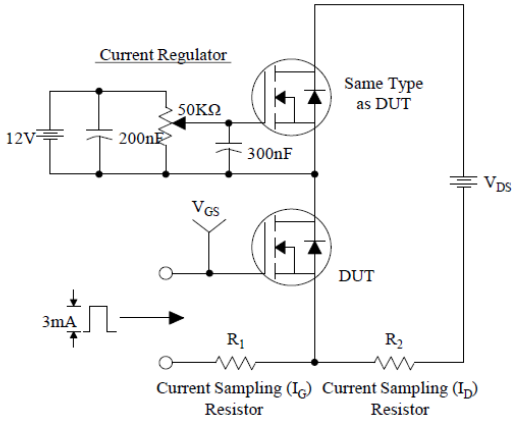
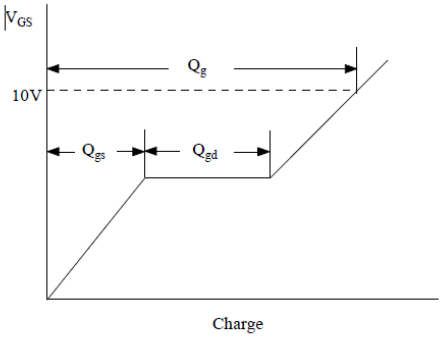


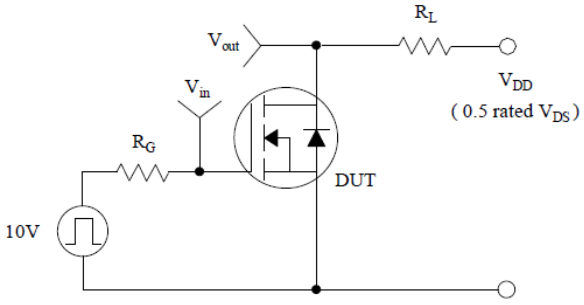
Figure 11-2. Transient Thermal Response Curve for JFFM9N50C

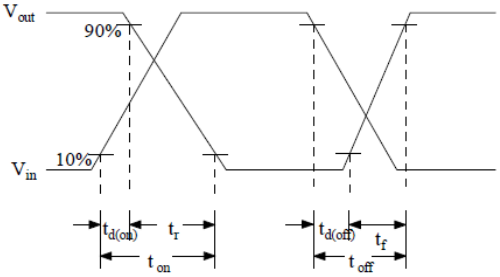
Test Circuit & Waveform



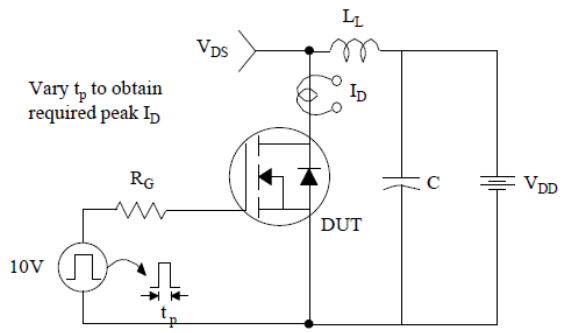


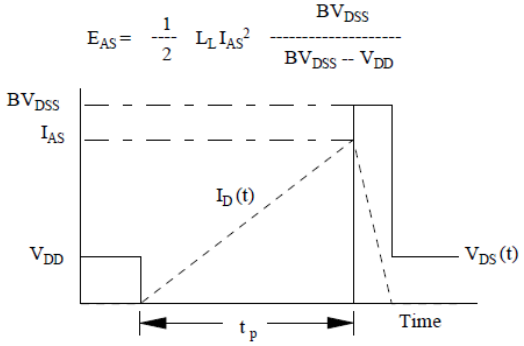
Gate Charge Test Circuit & Waveform





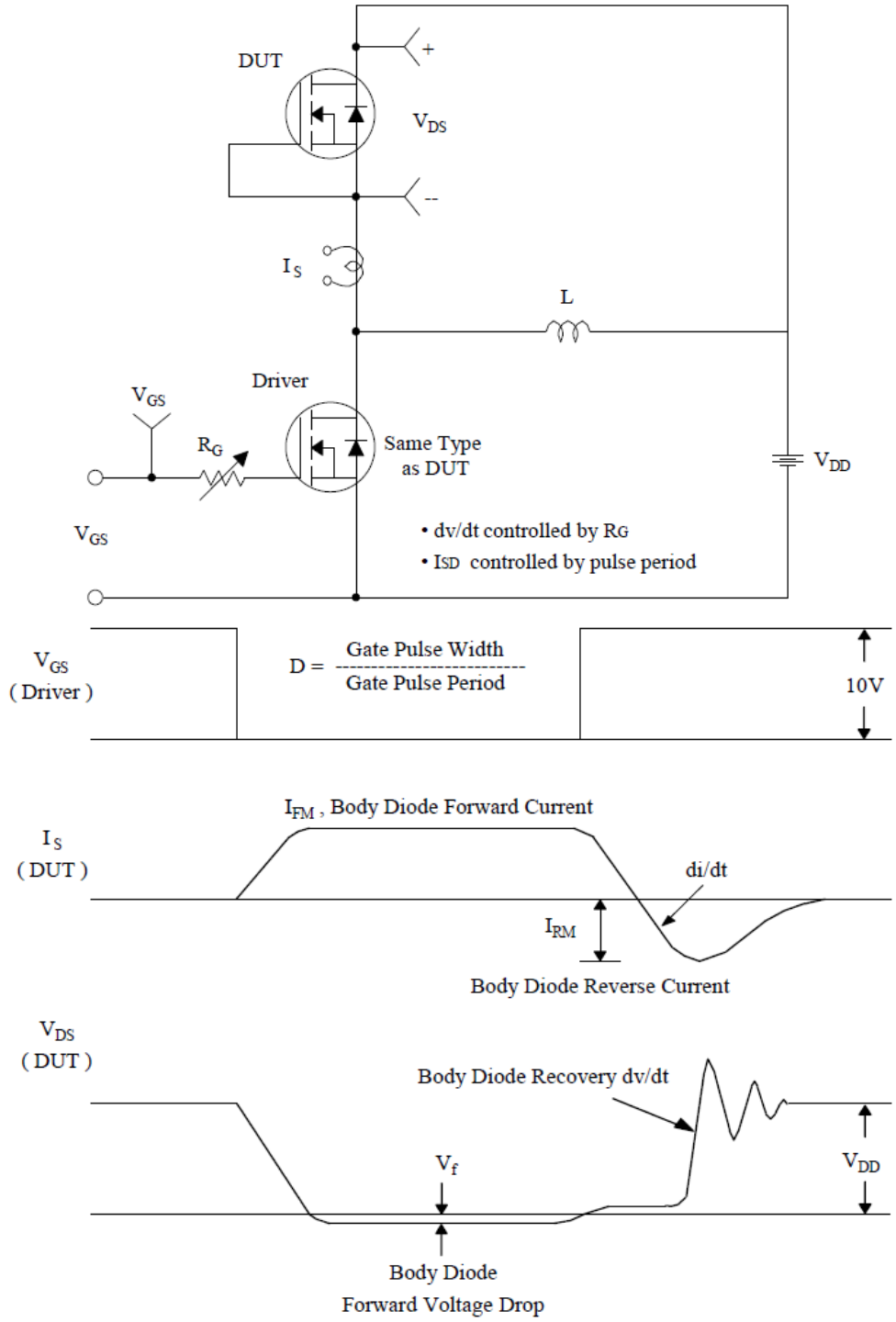
Resistive Switching Test Circuit & Waveforms





Unclamped Inductive Switching Test Circuit & Waveforms

Test Circuit & Waveform



Peak Diode Recovery dv/dt Test Circuit & Waveforms